31st EUROMICRO Conference on Software Engineering and Advanced Applications

8th EUROMICRO Conference on Digital System Design

EUROMICRO2005

PORTO, PORTUGAL, AUGUST 31st - SEPTEMBER 2nd, 2005

Contents

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Welcome Message

On behalf of the Local Organizing Committee it is my pleasure to welcome to Porto and to FEUP all participants of the 31st SEAA and 8th DSD EUROMICRO Conferences.

Porto is an old and active city, located in the north of Portugal, where the Douro River meets the Atlantic Ocean. Their inhabitants are known for their rugged and hard-working nature but also for their good spirits, their willingness to enjoy life, and their love for their city. It is our hope that this will help create the right setting for a fruitful event. One in which we can perform serious work in a relaxed atmosphere. One that promotes relevant exchanges of experiences and ideas, leading to the establishment of ties and networks that will last long after the three days of the Conference.

It is our hope that everything is in place to allow participants to extract the maximum benefit from the excellent technical program that was put together. The Conference Chairs (Ivica Crnkovic and Christophe Wolinski), the Tutorial Chair (Lech Jozwiak), the organizers of the Work in Progress Session (Gerhard Chroust, Erwin Grosspietch and Konrad Klöckner), are also names to be thanked for their work in assuring a program of high quality. To all authors and reviewers, to the session and track chairs, our thanks for their contribution and their effort. One final word of gratitude goes to the sponsors for their valuable support.

Welcome to Porto and to FEUP, the Faculty of Engineering of the University of Porto. Enjoy your work and have a pleasant stay.

José Silva Matos
Local Organization Chair

DSD Tutorial Day

August 30th, 2005

Registration
8.30 – 9.00 (Main Entrance)

Digital System Clocking: High-Performance and Low-Power Aspects
9.00 – 12.30 (Room B006)
: *Vojin G. Oklobdzija, University of California, Davis*
: *Vladimir M. Stojanovic, MIT*
: *Dejan M. Markovic University of California, Berkeley*
: *Nikola M. Nedovic, Fujitsu America Laboratories*

This tutorial provides up-to-date information on the most recent advances in the area of Digital System Clocking that has become one of the most important topics in the field of digital system design due to its high relevance to both High-Performance and Low-Power design.

1. Introduction
2. Theory of Clocked Storage Elements
3. Timing and Energy Parameters
4. Pipelining and Timing Analysis
5. High-Performance System Issues
6. Low-Energy System Issues
7. Simulation Techniques
8. State-of-the-Art Clocked Storage Elements in CMOS Technology
9. Microprocessor Examples

System-Level Performance Analysis
14:00 – 17:00 (Room B006)
Piet van der Putten, Bart Theelen and Jeroen Voeten
Eindhoven University of Technology, The Netherlands

This tutorial presents a system-level methodology for predicting the performance of industrial-sized embedded systems. Starting from UML specification, the methodology derives formal executable performance models expressed in POOSL. These models are transformed into Markov chains to support both analytical and simulation-based performance evaluation. After presenting the theoretical background of the methodology, participants are invited to experiment with the supporting tools through a modest case study. This research was supported by the Dutch Program for Research on Embedded Systems and Software (PROGRESS).

Keynote Speeches

August 31th, 2005

Software Process Improvement Considered Obsolete: A Transition from Improvement-in-the-Large to Improvement-in-the-Small
10:00 – 11:00 (Auditório)
Speaker: *Pekka Abrahamsson*

Multi-media Applications and Imprecise Computation
11:30 – 12:30 (Auditório)
Speaker: *Melvin A. Breuer*

September 1st, 2005

Components in Product Lines — The Next Steps
9:00 – 10:00 (Auditório)
Speaker: *Rob van Ommering*

SoC Design for Advanced Applications
10:00 – 11:00 (Auditório)
Speaker: *Bernard Candaele*

Wireless Sensor Systems — Constraints and Future Prospect
11:30 – 12:30 (Auditório)
Speaker: *Dirk Timmermann*

September 2nd, 2005

UML and Components for System Modelling
11:00 – 12:00 (Auditório)
Speaker: *François Terrier*

Networks on Chip
12:00 – 13:00 (Auditório)
Speaker: *Hannu Tenhunen*

31st SEAA Program Sessions

CBSE — COMPONENT-BASED SOFTWARE ENGINEERING
The Component-based Software Engineering (CBSE) track has a goal to point out the overall challenges and problems of the component-based approach, but also to show the new ideas, solutions and practices. The aim of the track is to bring together researchers and practitioners from academia and industry to improve the theories, technologies, and processes in component-based software development.

SPPI — SOFTWARE PROCESS AND PRODUCT IMPROVEMENT
Software process and product improvement (SPPI) aims at significantly increasing both the quality of systems and the productivity of software development. The SPPI conference track concentrates on processes, methods, and tools improving software quality.

MMTC — MULTIMEDIA & TELECOMMUNICATIONS
Regardless of different end-systems and the underlying network infrastructure, multimedia plays an important role in almost any application. These applications spread from collaborative environments to gaming applications and include also m-commerce. New middleware providing an abstraction layer for particular hardware like mobile phones, PDAs or wearables, and particular network services, as well as network requirements are key issues in this field.

August 31th, 2005

CBSE Session I — Component Models and Technologies
14:00 – 15:30 (B004)

: Developing Content-Intensive Applications with XML Documents, Document Transformations and Software Components
José L. Sierra, Alfredo Fernández-Valmayor, Baltasar Fernández-Manjón, Antonio Navarro

: Develop and Use Own Components Framework: Results and Expectations
Vladimir Lilov, Sylvia Ilieva

: Towards a Components Grouping Technique within a Domain Engineering Process
Ana Paula Blois, Cláudia Werner, Karin Becker

SPPI Session I — Case Studies and Experiences
Chair: Stefan Biffl
14:00 – 15:30 (Room B007)

: Processes Used During Software Integration & Experiences from Industry
Rikard Land, Ivica Crnkovic, Stig Larsson

: The Impact of Process Workshop Involvement on the Use of an Electronic Process Guide: A Case Study
Nils Brede Moe, Torgeir Dingøsyr

: The Introduction and Use of a Tailored Unified Process & a Case Study
Hans Westerheim, Geir Kjetil Hanssen

MMTC Session I — Quality of Service
14:00 – 15:30 (Room B005)

: Improving the Admissibility of Flows with Bounded Arrivals and Bounded Delay Requirements in Rate-controlled Packet Networks
Slim Abdellatif, Guy Juanole

: Virtual Dropping for Endpoint Admission Control
Torsten Braun, Matthias Scheidegger, Marco Studer

: Using Distributed Admission Control to Support Multimedia Applications in MANET Environments
Carlos T. Calafate, Pietro Manzoni, Manuel P. Malumbres

CBSE Session II — Component-based Modelling and Analysis
Chair: Kung-Kiu Lau
16:00 – 17:30 (B004)

: Fine-grained Contract Negotiation for Hierarchical Software Components
Philippe Collet, Hervé Chang

: Modelling of Input-Parameter Dependency for Performance Predictions of Component-Based Embedded Systems
Egor Bondarev, Peter de With, Michel Chaudron, Johan Musken

: Analyzing Component-Based Systems Using the Self-Organizing Map
Heikki Verta

SPPI Session II — Design Quality
Chair: Gerhard Chroust
16:00 – 17:30 (Room B007)

: Analyzing Software Architectures for Usability
Eelke Folmer, Jan Bosch

: Design Failure Cost as a Measure of a Process Measurement System
Karl W. Wagner, Walter Dürr

: Improvement of Design Specifications with Inspection and Testing
Dietmar Winkler, Stefan Biffl

MMTC Session II — Video Delivery
16:00 – 17:30 (Room B005)

: Distributed P2P Merging Policy to Decentralize the Multicasting Delivery
P. Hernández, A. Ripoll, R. Suppi, E. Luque

: User Behaviour Analysis of a Video-On-Demand Service with a Wide Variety of Subjects and Lengths
M. Vilas, X.G. Pañeda, R. García, D. Melendi, V.G. García

: A Hybrid Spatial-Temporal Fine Granular Scalable Coding for Adaptive QoS Internet Video
Chung-Ming Huang, Chung-Wei Lin

Special Session I — Next Generation of Web Computing
Chair: Konrad Klöckner
16:00 – 17:30 (Room B006)

: PRIMI & an Open Platform for the Rapid and Easy Development of Instant Messaging Infrastructures
Tom Gross, Christoph Oemig

: Evolution of Web Computing Systems: Experiences from Web-portal Projects
Andreas Billig, Jan Gottschick, Kurt Sandkuhl

: Interest Derivation Through Keywords
Michael Sonntag, Andreas Putzinger

: A Toolbar for Efficient Interaction in Online Communities
Sabine Kolvenbach, Wolfgang Gräther, Konrad Klöckner

September 1st, 2005

CBSE Session III — CB Software Architecture
Chair: Zoran Kalafatic
14:00 – 15:30 (Room B004)

: QoS-aware Mobile Middleware for Video Streaming
Sten L. Amundsen, Ketil Lund Carsten Griwodz, Pål Halvorsen

: A Framework to Specify Incremental Software Architecture Transformations
Anne-Francoise Le Meur, Olivier Barais, Laurence Duchien

: Enhancing the Management of a J2EE Application Server using a Component Based Architecture
Takoua Abdellatif-Berrayana

SPPI Session III — SPPI Methods
Chair: Erwin Grosspietsch
14:00 – 15:30 (Room B007)

: RUPSec: Extending Business Modeling and Requirements Disciplines of RUP for Developing Secure Systems
Pooya Jaferian, Golnaz Elahi, Mohammad Reza, Ayatollahzadeh Shirazi, Babak Sadeghiyan

: Software Security Analysis - Execution Phase Audit
Bengt Carlsson, Dejan Baca

: Multi-level Configuration Management with Fine-grained Units
Tien N. Nguyen, Ethan V. Munson, John T. Boyland, Cheng Thao

MMTC Session III — Traffic Engineering / /Accounting
14:00 – 15:30 (Room B005)

: Traffic Engineering from a Fiber To Service Area Access Network
Roberto García, Isabel Rodríguez, Víctor García, Xabiel G. Pañeda, David Melendi

: A Model for User Based Traffic Accounting
Ge Zhang, Bernd Reuther

: Network Traffic Analyzing and Monitoring Locations in the IP Multimedia Subsystem
Tomi Räty, Jouko Sankala, Markus Sihvonen

Special Session II — Model Development Engineering I.
Model-based/Component-based Development
Chair: Martin Törngren
14:00-15:30 (Room B006)

: A Tool for Reliability and Availability Prediction
Anne Immonen, Antti Niskanen

: UML-based Design of Network Processor Applications
A. Bertolino, G. De Angelis, R. Mirandola

: Component Based vs. Model Based Development: A Comparison in the Context of Vehicular
Martin Törngren, DeJiu Chen, Ivica Crnkovic

CBSE & SPPI Session IV — Component Classifications and Ontologies
Chair: Massimo Tivoli
16:00 – 17:30 (Room B004)

: QoSOnt: a QoS Ontology for Service-Centric Systems
Glen Dobson, Russell Lock, Ian Sommerville

: A Taxonomy of Software Component Models
Kung-Kiu Lau, Zheng Wang

: Component Assessment Metrics for CBSE
Miguel Goulão, Fernando Abreu

MMTC Session IV — Services
16:00 – 17:30 (Room B005)

: The Mobile Telecommunications Industry: the Competition Under the Hypothesis of Price Discrimination Strategy
Livio Cricelli, Francesca Di Pillo, Massimo Gastaldi, Nathan Levialdi

: Nested Uniform Resource Identifiers
Manuel Uruña, David Larrabeiti

: Voice over IP - Considerations for a Next Generation Architecture
Markus Hillenbrand, Joachim Götze, Paul Müller

Special Session III — Model Development Engineering II — Modelling and Tools
Chair: Marcus Alanen
16:00-17:30 (Room B006)

: A Model and Tool Integration Platform for Multi-Disciplinary Development
Jad El-khoury, Ola Redell, Martin Tørngren

: Model Interchange Using OMG Standards
Marcus Alanen, Ivan Porres

September 2nd, 2005

CBSE Session V — Dependable Component-based Systems
Chair: Michel Chaudron
9:00 – 10:30 (Room B004)

: Software Component Certification: A Survey
Alexandre Álvaro, Eduardo Santana de Almeida, Sílvio Romero de Lemos Meira

: Surviving Errors in Component-Based Software
Titos Saridakis

: Robocop: A Robust Component Model for Resource Constrained Devices
Hugh Maaskant (Invited Speaker)

SPPI Session V — Agile Methods
Chair: Rudolf Ramler
9:00 – 10:30 (Room B007)

: From Agile Software Development to Agile Businesses
Christoph Steindl

: Agile Procurement: New Acquisition Approach to Agile Software Development
Diane Jamieson, Kevin Vinsen, Guy Callender

: Naked Objects versus Traditional Mobile Platform Development: A Comparative Case Study
Heikki Keränen, Pekka Abrahamsson

MMTC Session V — Architectures
9:00 – 10:30 (Room B005)

: RSerPool a Protocol for Fault-tolerant Session Layer
Thomas Dreibholz, Erwin P. Rathgeb

: ASQue: An Agent Communication Language for Ad-hoc Wireless Sensor Networks
S.N.I. Mount, R.M. Newman, S.R. Lakin, R.J. Low, E.I. Gaura

CBSE Session VI — Emerging Technologies
14:30 – 16:00 (Room B004)

: Patterns and Component-Oriented System Development
John Hutchinson, Gerald Kotonya

: The Audition Framework for Testing Web Services Interoperability
Andrea Polini, Antonia Bertolino

: Distribution of a Hierarchical Component in a Non-Connected Environment
Didier Hoareau, Yves Maheo

SPPI Session VI — Process Improvement
Chair: Walter Dürr
14:30 – 16:00 (Room B007)

: Encouraging Self-Organization: Reflections on a Quality Improvement Workshop
Ramler Rudolf, Dagmar Auer

: An Outline of an Emergency Maintenance Process Model
Mira Kajko-Mattsson, Per Winther, Brian Vang, Anne Petersen

Work in Progress I
14:30 – 16:00 (Room B006)

: Towards a Software Component Quality Model
Alexandre Álvaro, Eduardo Santana de Almeida, Sílvio Romero de Lemos Meira

: A Comparison of SPA Methods
Alberto Sampaio, Edwin M. Gray, Fernando M. Martins

: ProjectIT-Time: Integrated Management, Evaluation and Measurement of Information Systems Projects
Paula Ventura Martins, Alberto Rodrigues da Silva

: Towards a Model-Driven Reuse Process
Daniel Lucrédio, Renata P. M. Fortes, Alexandre Álvaro, Eduardo Santana de Almeida, Sílvio R. L. Meira

: Towards Code Layout Improvement Through Dynamic Basic-Block Motion
Ricardo Gonçalves Quintão, Valmir C. Barbosa, Edil S. T. Fernandes

: Linearization of the Logic Functions Defined in SOP Form
Osnat Keren, Ilya Levin

: HTracer: A Dynamic Instruction Stream Research Tool
Michael Hicks, Colin Egan, Bruce Christianson, Patrick Quick

: Using Event Logs in System Dependability Evaluation
Janusz Sosnowski, M. Poleszak

: Fail-Safe System Architectures
Radek Dobias, Hana Kubatova

CBSE & SPPI Session VII — Component Development Process
Chair: Raul Vidal
16:30 – 18:00 (Room B004)

: A Hybrid Component-Based System Development Process
Egon Teiniker, Gernot Schmoelzer, Christian Kreiner, Joerg Faschingbaue

: How Agile COTS Selection Methods are (and can be)?
Xavier Franch, Fredy Navarrete, Botella Pere

: Visual Assessment Techniques for Component-Based Framework Evolution
Lucian Voinea

Work in Progress II
16:30 – 17:00 (Room B006)

: NSI: a Component Model for Legacy Software in Consumer Electronics
Valentine Ogier-Galland, Cédric Hombourger

: An Embedded Implementation of the Microsoft Common Language Infrastructure
Joey C. Libby, Kenneth Kent

: Monitoring the Ocean Environment with Large-Area Wireless Sensor Networks
Frank Reichenbach, Matthias Handy, Dirk Timmermann

31st EUROMICRO Conference **on Software Engineering and Advanced Applications**

8th EUROMICRO Conference **on Digital System Design**

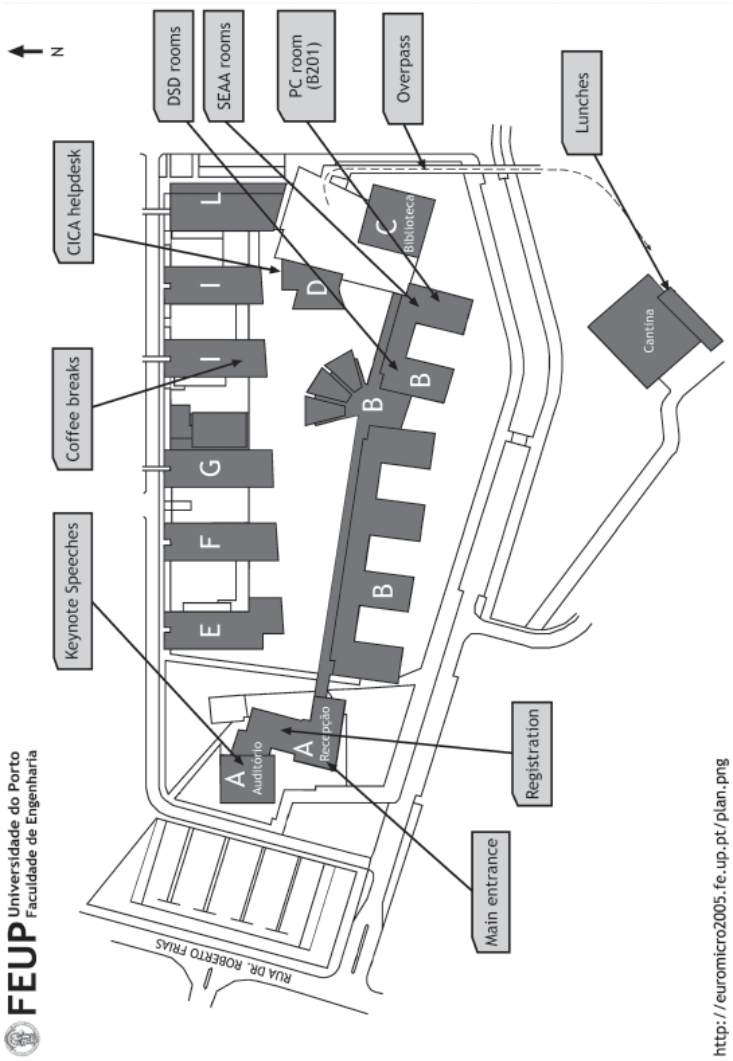
31st SEAA Program Overview

Wednesday, August 31st				
8:30-9:30	Registration			
9:30-10:00	Opening Session			
10:00-11:00	Keynote speech (Auditório): Pekka Abrahamsson - Software Process Improvement Considered Obsolete: A Transition from Improvement-in-the-Large to Improvement-in-the-Small			
11:00-11:30	Coffee Break			
11:30-12:30	Keynote speech (Auditório): Melvin A. Breuer - Multi-media Applications and Imprecise Computation			
12:30-14:00	Lunch			
14:00-15:30	CBSE I (B004): *Component Models and Technologies*	SPPI I (B007): *Case Studies and Experiences*	MMTC I (B005): *Quality of Service*	
15:30-16:00	Coffee Break			
16:00-17:30	CBSE II (B004): *Component-based Modelling and Analysis*	SPPI II (B007): *Design Quality*	MMTC II (B005): *Video Delivery*	Special Session I (B006): *Next Generation of Web Computing*
18:00	Cocktail/Reception			
Thursday, September 1st				
9:00-10:00	Keynote speech (Auditório): Rob van Ommering - *Components in Product Lines — The Next Steps*			
10:00-11:00	Keynote speech (Auditório): Bernard Candaele - *SoC Design for Advanced Applications*			
11:00-11:30	Coffee Break			
11:30-12:30	Keynote speech (Auditório): Dirk Timmermann - Wireless Sensor Systems — Constraints and Future Prospect			
12:30-14:00	Lunch			
14:00-15:30	CBSE III (B004): *Component-based Software Architecture*	SPPI III (B007): *SPPI Methods*	MMTC III (B005): *Traffic Engineering / Accounting*	Special Session II (B006): *Model Driven Engineering I*
15:30-16:00	Coffee Break			
16:00-17:30	CBSE & SPPI IV(B004): *Component Classifications and Ontologies*		MMTC IV (B005): *Services*	Special Session III (B006): *Model Driven Engineering II*
20:00	Conference Dinner			
Friday, September 2nd				
9:00-10:30	CBSE V (B004): *Dependable Component-based Systems*	SPPI V (B007): *Agile Methods*	MMTC V (B005): *Architectures*	
10:30-11:00	Coffee Break			
11:00-12:00	Keynote speech (Auditório): François Terrier - *UML and Components for System Modelling*			
12:00-13:00	Keynote speech (Auditório): Hannu Tenhunen - *Networks on Chip*			
13:00-14:30	Lunch			
14:30-16:00	CBSE VI (B004): *Emerging Technologies*	SPPI VI (B007): *Process Improvement*		Work in Progress I (B006)
16:00-16:30	Coffee Break			
16:30-18:00	CBSE & SPPI VII (B004): *Component Development Process*			Work in Progress II (B006)

8th DSD Program Overview

Wednesday, August 31st				
8:30-9:30	Registration			
9:30-10:00	Opening Session			
10:00-11:00	Keynote speech (Auditório): Pekka Abrahamsson - *Software Process Improvement Considered Obsolete: A Transition from Improvement-in-the-Large to Improvement-in-the-Small*			
11:00-11:30	Coffee Break			
11:30-12:30	Keynote speech (Auditório): Melvin A. Breuer - *Multi-media Applications and Imprecise Computation*			
12:30-14:00	Lunch			
14:00-15:00	S1 (B010): SS2. *Dependability and Testing of Digital Systems. Part 1*	S2 (B013): System Synthesis. *Part 1. Power Driven System Synthesis*	S3 (B011) Circuits Synthesis. *Part 1. Arithmetic*	
15:00-15:30	Coffee Break			
15:30-17:10	S4 (B010): Dependability and Testing of Digital Systems. *Part 2*	S5 (B013): System Synthesis. *Part 2. Component Based System Synthesis*	S6 (B011): Circuits Synthesis. *Part 2. Logic Synthesis*	
17:15-17:30	Poster Session			
18:00	Cocktail/Reception			
Thursday, September 1st				
9:00-10:00	Keynote speech (Auditório): Rob van Ommering - *Components in Product Lines — The Next Steps*			
10:00-11:00	Keynote speech (Auditório): Bernard Candaele - *SoC Design for Advanced Applications*			
11:00-11:30	Coffee Break			
11:30-12:30	Keynote speech (Auditório): Dirk Timmermann - *Wireless Sensor Systems — Constraints and Future Prospect*			
12:30-14:00	Lunch			
14:00-15:20	S7 (B010): SS1.: Wireless Sensor *Systems. Part 1*	S8 (B013): Verification Techniques. *Part 1*	S9 (B011): Application Specific Architectures. *Part 1*	
15:30-16:00	Coffee Break + Poster Session			
16:00-17:30	S10 (B010): SS1. Wireless Sensor Systems. *Part 2*	S11 (B013): Verification Techniques. *Part 2*	S12 (B011): Application Specific Architectures. *Part 2*	
20:00	Conference Dinner			
Friday, September 2nd				
9:00-10:30	S13 (B010): System Synthesis. Part 3. *High Level Language-based System Synthesis*	S14 (B013): Reconfigurable Systems. *Part 1*	S15 (B011): Data Management in SoC. *Part 1*	
10:30-11:00	Coffee Break + Poster Session			
11:00-12:00	Keynote speech (Auditório): François Terrier - *UML and Components for System Modelling*			
12:00-13:00	Keynote speech (Auditório): Hannu Tenhunen - *Networks on Chip*			
13:00-14:30	Lunch			
14:30-16:30	S16 (B010): SS3. Remote Educational Tools for Design and Testing. *Part 1*	S17 (B013): Circuits Synthesis. *Part 3. Advanced Logic Synthesis*	S18 (B011): Performance Optimization: Architecture and Tools. *Part 1*	WP1 (B012): Work in Progress I
16:30-17:00	Coffee Break			
17:00-18:30				WP2 (B012): Work in Progress II

Plan of FEUP



8th DSD Program Sessions

August 31th, 2005

S1 — SS2: Dependability and Testing of Digital Systems, Part 1
Chair: H. Kubatova
14:00-15:00 (Room B010)

: Bist Technique for GALS Systems
Milos Krstic, Eckhard Grass

: Functional Vectors Generation for RT-Level Verilog Descriptions Based on Path Enumeration and Constraint Logic Programming
Tun Li, Dan Zhu, Yang Guo, SiKun Li

S2 — System Synthesis, Part 1. Power Driven System Synthesis
Chair: L. Fanucci
14:00-15:00 (Room B013)

: An Innovative MDA Methodology for Embedded Real-time System
A. Cuccuru, R. De Simone, T. Saunier, G. Siegel, Y. Sorel

: Power-Composition Profile Driven Co-Synthesis with Power Management Selection for Dynamic and Leakage Energy Reduction
Dong Wu, Bashir M Al-Hashimi, Marcus Schmitz, Petru Eles

S3 — Circuit Synthesis, Part 1. Arithmetic
Chair: T. Sasao
14:00-15:00 (Room B011)

: A Low-Power FIR Filter Using Combined Residue and Radix-2 Signed-Digit Representation
Andreas Lindahl, Lars Bengtsson

: Approximating Trigonometric Functions with the Laws of Sines and Cosines using the Logarithmic Number System
Mark G Arnold

S4 — SS2: Dependability and Testing of Digital Systems, Part 2
Chair: H. Kubatova
15:30-17:10 (Room B010)

: Improvement of the Fault Coverage of the Pseudo-Random Phase in Column Matching BIST
Petr Fiser, Hana Kubatova

: Characterization of Wavelet-based Image Coding Systems for Algorithmic Fault Detection
Lucía Costas Perez, Juan J. Rodríguez-Andina

: Improved Fault Emulation for Synchronous Sequential Circuits
J. Raik, P. Ellervee, V. Tihhomirov, R. Ubar

: Defect-Oriented Test-and Layout-Generation for Standard-Cell ASIC Designs
J. Sudbrock, J. Raik, R. Ubar, W. Kuzmicz, W. Pleskacz

: Power-Constrained Hybrid BIST Test Scheduling in an Abort-on-First-Fail Test Environment
Zhiyuan He, Gert Jervan, Zebo Peng, Petru Eles

S5 — System Synthesis, Part 2. Component Based System Synthesis
Chair: K. Waldschmidt
15:30-17:00 (Room B013)

: Hardware Design Based on Virtual Component Synthesis
A. Fouilliart, N. Abdelli, E. Casseau, B. Le Gall, Ch. Jego, N. Heno

: High-Level Synthesis for DVB-DSNG Modem in an Optimized Latency Insensitive System Context
N. Abdelli, P. Bomel, P. Kajfasz, E. Martin, E. Boutillon, A. Fouilliart

: Embedded Object Architecture
Tero Vallius, Juha Röning

: An Effective Framework for Enabling the Reuse of External Soft IP
Soujanna Sarkar, Subash Chandar G.

S6 — Circuit Synthesis, Part 2. Logic Synthesis
Chair: T. Luba
15:30-16:40 (Room B011)

: A Novel Method of Two-stage Decomposition Dedicated for PAL-based CPLDs
Dariusz Kania, Józef Kulisz, Adam Milik

: An Advanced Minimization Technique for Multiple Valued Multiple Output Logic Expressions Using LUT and Realization Using Current Mode CMOS
Md.S. Shahriar, M.A.R. Mustafa, et al.

: State Assignment for PAL-based CPLDs
Robert Czerwinski, Dariusz Kania

: Coefficient Bit Reordering Method for Configurable FIR Filtering on Folded Bit-plane Array
Vladimir Ciric, Ivan Milentijevic

: Automatic Design of Binary and Multiple-Valued Logic Gates on the RTD Series
Krzysztof S. Berezowski, Sarma B.K. Vrudhula

Poster Session 1
17:20-17:35 (Building B)

September 1st, 2005

S7 — SS1: Wireless Sensor Systems, Part 1
Chair: Matthias Handy
14:00-15:15 (Room B010)

: Design of Transport Triggered Architecture Processors for Wireless Encryption
P. Hämäläinen, J. Heikkinen, M. Hännikäinen, T. Hämäläinen

: Mixed Signal CMOS Circuits for Ad-Hoc Networks (Invited paper)
C. Siu, K. Iniewski, F. Nabky, M. El-Gamal, K. Townsend, J. Haslett

: Co-simulation of Wireless Local Area Network Terminals with Protocol Software Implemented in SDL
Petri Kukkala, Marko Hännikäinen, Timo D. Hämäläinen

: Optimization of Electronic Power Consumption in Wireless Sensor Nodes
Y. Manoli, S.K. Ramachandran, S.K. Jayapal, R. Bhutada, R. Huang

: Vital Signs Remote Management System for PDA
Danielly Cruz, Edna Barros

S8 — Verification Techniques
Chair: S. Ruelke
14:00-15:10 (Room B013)

: MA2TG: A Functional Test Program Generator for Microprocessor Verification
Tun Li, Dan Zhu, Yang Guo, SiKun Li

: A Processor for Testing Mixed-signal Cores in System-on-Chip
F. Duarte, J. Machado Silva, José C. Alves,J. Matos

: Functional Test Generation Remote Tool
E. Bareisa, V. Jusas, K. Motiejunas, R. Seinauskas

: Validation of Embedded Systems using Formal Method-aided Simulation
Daniel Karlsson, Petru Eles, Zebo Peng

S9 — Application Specific Architectures, Part 1
Chair: J. Sosnowski
14:00-15:20 (Room B011)

: VLSI Design of a High-Throughput Multi-Rate Decoder for Structured LDPC Codes
M. Rovini, Nicola E. L'Insalata, F. Rossi, Luca Fanucci

: A FPGA Based Design of a Multiplierless and Fully Pipelined JPEG Compressor
L.V. Agostini, R.E. Carvalho Porto, I. Saraiva Silva, S. Bampi

: Reconfigurable Parallel Approximate String Matching on FPGAs
Jin Hwan Park

: Efficient MLP Digital Implementation on FPGA
S. Vitabile, V. Conti, F. Gennaro, F. Sorbello

: Designing a Binary Neural Network Co-processor
Michael Freeman, Jim Austin

: Efficient Host-Independent Coprocessor Architecture for Speech Coding Algorithms
H. Safizadeh, H. Noori, M. Sedighi, A. Jahanian, N. Zolfaghari

: Massively Parallel Hardware Architecture for Genetic Algorithms
Nadia Nedjah, Luiza de Macedo Mourelle

: Implementation of a Block Based Neural Branch Predictor
Oswaldo Cadenas, Graham Megson, Daniel Jones

: PRUS - Processor Network for Digital Circuit Implementation
S. Hyduke, V. Hahanov, V. Obrizan, O. Guz

: Capturing Processor Architectures from Protocol Processing Applications: a Case Study
Seppo Virtanen, Jani Paakkulainen, Tero Nurmi

: Yield-aware Floorplanning
Zhaojun Wo, Israel Koren, Maciej Ciesielski

Poster Session 2
15:30-16:00 (Building B)

S10 — SS1: Wireless Sensor Systems, Part 2
Chair: Matthias Handy
16:00-17:30 (Room B010)

: Design of a Development Platform for HW/SW Codesign of Wireless Integrated Sensor Nodes
K. Virk, M. Leopold, A. Vad Lorentzen, M. Hansen, P. Bonnet, J. Madsen

: An Efficient MAC Protocol for Sensor Network Considering Energy Consumption and Information Retrieval
Yashar Ghiassi, Mohammad Mehdi Mansouri

: Wireless Sensor Network Implementation for Industrial Linear Position Metering
Mikko Kohvakka, Marko Hännikäinen, Timo D. Hämäläinen

S11 — Verification Techniques, Part 2
16:00-17:30 (Room B013)

: MemBIST Applet for Learning Principles of Memory Testing and Generating a BIST Structure
Maria Fischerova, Martin Simlastik

: High-Level Modelling and Detection of the Faulty Behaviour of VOQ Switches under Balanced Traffic
Miguel Pereira-Varela, Enrique Soto-Campos, Juan J. Rodriguez

: Delay Testability Properties of Circuits Realizing Threshold Functions and Symmetric Functions
Piotr Patronik

S12 — Application Specific Architectures, Part 2
Chair: F. Leporati
16:00-17:30 (Room B011)

: A New Architecture for Fast Arithmetic Coding in H.264 Advanced Video Coder
Roberto R. Osorio, Javier D. Bruguera

: Exploring Graphics Processor Performance for General Purpose Applications
Pedro Trancoso, Maria Charalambous

: Hardware-Based Implementation of the Common Approximate Substring Algorithm
Kenneth B. Kent, Sharon Van Schaick, J.E. Rice, P.A. Evan

September 2nd, 2005

S13 — System Synthesis, Part 3. High Level Language based System Synthesis
Chair: K. Judmann
9:00-10:25 (Room B010)

: Cost-effective VLSI Design of Non Linear Image Processing Filters
S. Saponara, M. Cassiano, S. Marsi, R. Coen, L. Fanucci

: Java to Hardware Compilation for non Data Flow Applications
Per Andersson, Krzysztof Kuchcinski

: Formal Communication Semantics of SysetmC {FL}
K.L. Man

: A high-level Tool for the Design of Custom Image Processing Systems
Sérgio Martins, José C. Alves

: Processing of Streams on Multiprocessor Architecture
Nikolay Kavaldjiev, Gerard J.M. Smit, Pierre G. Jansen

S14 — Reconfigurable Systems, Part 1
Chair: A. Nunez
9:00-10:25 (Room B013)

: A Constraints Programming Approach for Fabric Cell Synthesis
C. Wolinski, K. Kuchcinski

: SystemC-based Design Methodology for Reconfigurable System-on-Chip
Yang Qu, Kari Tiensyrjä, Juha-Pekka Soininen

: Reducing Inter-configuration Memory Usage and Performance Improvement in Reconfigurable Computing Systems
Farhad Mehdipour, Morteza Saheb Zamani, Mehdi Sedighi

: An Adaptive On-line HW/SW Partitioning for Soft Real Time Reconfigurable Systems
G. Fakhreddine, A. Michel, A. Mohamed, B. Jemaa Maher

: Using a Tightly-coupled Pipeline in Dynamically Reconfigurable Platform FPGAs
Miguel L. Silva, João Canas Ferreira

S15 — Data Management in SoC, Part 1
Chair: J.S. Matos
9:00-10:30 (Room B011)

: Predictable Embedding of Large Data Structures in Multiprocessor Networks-on-chip
Stuijk, Geilen, Basten, Mesman

: An Approach to Execute Conditional Branches onto SIMD Multi-Context Reconfigurable Architectures
F. Alexander R. Velez, M.S. Martin, M.F. Centeno, N. Bagherzadeh

: Optimization of a Bus-based Test Data Transportation Mechanism in System-on-Chip
Anders Larsson, Erik Larsson, Petru Eles, Zebo Peng

Poster Session 3
10:30-11:00 (Building B)

S16 — SS3: Remote Educational Tools for Design and Testing, Part 1
Chair: R. Ubar
14:30-16:00 (Room B010)

: An Educational Environment for Digital Testing: Hardware, Tools, and Web-Based Runtime Platform
Jaan Raik, Raimund Ubar

: Educational Tool for the Demonstration of DfT Principles Based on Scan Methodologies
Josef Strnadel, Zdenek Kotasek

: Remote Path Delay Fault Simulation
Øystein Gjermundnes, Einar J. Aas

: Internet-based IC Technology Design and Simulation
V. Nelayev, V. Stempitsky, K. Kudin]

S17 — Circuit Synthesis, Part 3. Advanced Logic Synthesis
14:30-16:30 (Room B013)

: Decomposition of Multi-Output Functions for CPLDs
Dariusz Kania, Jozef Kulisz

: High-quality Sub-function Construction in the Information-driven Circuit Synthesis with Gates
Lech Jó Wiak, Szymon Biegaski

: Efficient Implementation of Digital Filters with Use of Advanced Synthesis Methods Targeted FPGA Architectures
M. Rawski, P. Tomaszewicz, H. Selvaraj, T. Luba

: On LUT Cascade Realizations of FIR Filters
Tsutomu Sasao, Yukihiro Iguchi, Takahiro Suzuki

S18 — Performance Optimization: Architecture and Tools, Part 1
Chair: K. Kuchcinski
14:30-16:00 (Room B011)

: Run-time Adaptive Resource Allocation and Balancing on Nanoprocessors Arrays
Danilo Pani, Giuseppe Passino, Luigi Raffo

: ARPA - A Technology Independent and Synthetizable System-on-Chip Model for Real-Time Applications
A.S.R. Oliveira, V.A. Sklyarov, A.B. Ferrari

: Dynamic Split: Flexible Border Between Instruction and Data Cache
Pedro Trancoso

Notes

Work in Progress I
14:30-16:00 (Room B012)

: Channel Widening Effect on the Effective Output Resistance of Deep-Submicron CMOS Line Driver and Its Application to Repeater Insertion
Andrea Pugliese, Franco Corapi, Gregorio Cappuccino

: Modeling of Total Parameter Variations
Frank Sill, Dirk Timmermann

: Enhancing the I-cache to Reduce the Power Consumption of Dynamic Branch Predictors
Colin Egan, Michael Hicks, Bruce Christianson, Patrick Quick

: Achieving Optimal Circuit Performance of Synthesis For Large Bit Size Adders
Weng Fook Lee, Ali Yeon

: Multiplier Execution Latency Reduction Using Variable Latency Pipeline
Tomáš Marek, Alois Pluháček

: Design of Optimized Reconfigurable HW Tasks using Operation Graph Signatures
Maik Boden, Steffen Rülke, Jürgen Becker

: Reconfigurable Duplex System Increasing Fault Tolerance for Circuits Based on FPGAs
Pavel Kubalík, Hana Kubátová

: On the Petri Net Based Test Scheduling
Richard Ruzicka

: Hardware Acceleration of Information Retrieval
Michael Freeman

Work in Progress II
16:30-17:30 (Room B012)

: Logarithmic Arithmetic for N-body Simulations
Mark Arnold, Philip Leong

: Periodic Licensing of FPGA based Intellectual Property
Nathaniel Couture, Kenneth B. Kent

: Packet Classification with Evolvable Hardware Hash Functions
Harald Widiger, Mathias Handy, Dirk Timmermann

: Developing an Ubiquitous Computing Demonstrator
Michael Freeman, Chris Bailey

: Efficient Data Feeding for Smart Vision System
G. Danese, M. Giachero, F. Leporati, N. D. Nazzicari, A. Sartori

: Implementing the Styx Network Protocol in Hardware
Ameet Patil, Michael Freeman, Rui Gao, Chris Bailey

Local Facilities

Coffee breaks
All coffee breaks will take place in room I-105 in building I (please see the plan).

Lunch
Lunch will take place in the Cantina (cafeteria). Please use the overpass near the Biblioteca (library) to cross the street (see the plan).

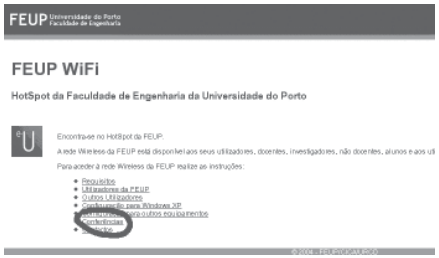
Internet
FEUP will provide Internet access for all participants in Euromicro2005.

Computer Room
Computers in room B201 may be used between 8:00 and 18:00. Login and password will be supplied to conference participants and the domain “FEUPSIG” must be used to login, as shown in the screen bellow.

Wireless Access
The wireless network “guest-e-U” can be used to access HTTP and HTTPS protocols.
Login and password will be supplied to conference participants.

Use the following procedure to establish a connection:

1) In the screen below choose “Conferências”.



2) In the next screen choose “Login”.

3) Finally, in the third screen fill the login and password supplied and then press “ENTRAR”.

In case of problems please contact the Helpdesk at CICA (Building D).

Social Events

Reception

A reception will be offered by the City Council to conference participants at the end of the first day. The event will take place in a 17th century building, called “Palácio do Freixo” (Freixo Palace). Buses will be available to take the participants from FEUP to the location of the event.

Palácio Freixo
Estrada Nacional 108, nº 206
4300-316 Porto

Dinner

The conference dinner will take place on September 1st at Taylor’s port wine cellars. Buses will be available to take the participants to the location of the event.

Caves Taylor’s
Rua do Choupelo, 250
4400-088 Vila Nova de Gaia
Tel.: 223 742 800

Faculdade de Engenharia da Universidade do Porto
Concepção gráfica: DCI - Agosto 2005